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V.S.

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
08/818,053	03/14/97	DEVIC G	0548-VDSK

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EXAMINER	
TUNG, K	
ART UNIT	**PAPER NUMBER**
2773	10

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Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applicant(s)
08/818,053	Devic
Examiner	**Group Art Unit**
K. Tung	2776

—The MAILING DATE of this communication appears on the cover sheet beneath the correspondence address—

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, such period shall, by default, expire SIX (6) MONTHS from the mailing date of this communication .
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

☒ Responsive to communication(s) filed on 3-8-99.

☒ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 1 1; 453 O.G. 213.

Disposition of Claims

☑ Claim(s) 10 – 24 is/are pending in the application.

Of the above claim(s)_____ is/are withdrawn from consideration.

☐ Claim(s)_____ is/are allowed.

☒ Claim(s) 10 - 24 is/are rejected.

☐ Claim(s)_____ is/are objected to.

☐ Claim(s)_____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☒ The proposed drawing correction, filed on 3/8/99 is ☑ approved ☐ disapproved.

☐ The drawing(s) filed on_____ is/are objected to by the Examiner.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119 (a)-(d)

☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 11 9(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number)_____.

☐ received in this national stage application from the International Bureau (PCT Rule 1 7.2(a)).

*Certified copies not received:_____.

Attachment(s)

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s)._____

☐ Interview Summary, PTO-413

☐ Notice of Reference(s) Cited, PTO-892

☐ Notice of Informal Patent Application, PTO-152

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Other_____

Office Action Summary

DETAILED ACTION

1. The amednment filed 3/8/99 has been considered in preparing this Office action.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371© of this title before the invention thereof by the applicant for patent.

3. Claims 10-20 are rejected under 35 U.S.C. § 102(e) as being anticipated by Larson et al (5,793,386).

As per claim 10, Larson et al teaches a graphics system (Fig. 1) for processing parameter values of graphics primitives in a display list, the graphics system comprising a plurality of register files (Fig. 2, 150) for storing a plurality of parameter values representing graphics primitives defined in the display list; and a graphics processor (Fig. 2, 135) coupled to the plurality of register files, wherein the graphics processor generates and processes a shortened display list (col. 5, lines 48-49) to enable faster processing of the graphics primitives, while maintaining the display quality of primitives displayed in a display unit, the graphics processor processing load instructions representative of a shortened display list instruction including the fetching of parameters associated

with the shortened display list instruction and storing fetched parameters randomly in the plurality of register files (abstract, lines 4-7). Therefore, claim 10 is anticipated by Larson et al.

As per claim 11, Larson et al teaches an instruction fetch logic unit (110) for fetching the next parameter values responsive to a graphics primitive to be displayed (col. 5, lines 25-44 and col. 6, lines 33-35).

As per claim 12, Larson et al teaches a load instruction unit (115) for storing load instructions representative of a shortened display list instruction, said load instruction comprising a plurality of data bits each of said plurality of data bits representing specific load functions to be performed by the load instruction (col. 5, line 27).

As per claim 13, Larson et al further teaches an opcode storage unit for storing opcode information responsive to each of the load instructions for determining the type of function to be performed by the graphics primitive to be rendered (col. 6, lines 45-46 and lines 65-68).

As per claim 14, Larson et al further teaches a write enable storage portion for storing write enable data for determining whether to load one of the plurality of registers in the register file (inherent by the teaching from col. 5, line 66 to col. 6, line 5).

As per claim 15, Larson et al further teaches an instruction partition portion for storing partition data for referencing the partition table to load parameter values to the referenced register (col. 2, Table I and from col. 6, line 41 to col. 8, line 18).

As per claim 16, Larson et al teaches a data shifter coupled to the load instruction unit for sequentially shifting data bits corresponding to a load instruction in order to write the load instructions to the register files (inherent by the re-order logic 250, col. 14, lines 57-61).

As per claim 17, Larson et al further teaches an address counter coupled to the register files for sequentially counting the address offsets of the register files locations as the load instruction data is loaded into the register files (register address generator 225).

As per claim 18, Larson et al further teaches a partition table coupled to the load instruction unit for storing the address offset bits corresponding to random register locations in the register files for the display parameter values in the display list (col. 2, Table I).

As per claim 19, Larson et al further teaches a write enable signal coupled to the address bit shifter, said write enable signal asserted high to allow the graphics processor to write the load instructions to the register files, wherein the write enable signal enables the graphics processor to randomly load register locations in the register file (inherent by the teaching of col. 5, line 66 to col. 6, line 5).

As per claim 20, Larson et al further teaches a request next parameter value signal coupled to the fetch logic unit, said request next parameter signal asserted high to allow the next parameter value in the display list to be fetched by the graphics processor (col. 6, lines 31-35).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 21-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Larson et al (5,793,386).

The teachings of Larson et al are given in previous paragraph of this office action. However, Larson et al fails to explicitly teach the partition look-up table comprises 64 entries of address offsets to the register file. It would have been obvious to one of ordinary skill in the art at the time the present invention was made to implement the teachings of Larson et al because the number of entries for the table are always power of 2 and to choose 64 is merely a matter of design choice without more. Therefore, claim 21 would have been obvious.

Claim 22 further requires the 64 entries of the partition table are evenly distributed to corresponding register locations in the register file which also would have been obvious for the reason given above with respect to claim 21 in order to properly address the register files.

Claim 23 further requires each of the 64 entries of the partition table is 6 binary wide which would have been obvious in view of the 64 entries because 64 is 2 to the power of 6.

Claim 24 further requires the register file comprises 1024 entries of addresses which would have been obvious for the reasons given above with respect to claim 21.

Response to Arguments

6. Applicant's arguments filed 3/8/99 have been fully considered but they are not persuasive.

Applicant's arguments are summarized at page 13. Applicant argues that the claimed invention is not shown by Larson et al for a number of reasons.

First, applicant argues that the lack of similar structure as noted above including the processor that retrieves and stores **only the necessary values** for the primitive, thereby minimizing the data required to pass over the system bus. The examiner disagrees because Larson et al suggests that "a host processor generates a display list that includes **only the values necessary** for rendering a primitive. The graphics controller (or processor) includes a **register file for receiving the display list**." (Abstract).

Second, applicant argues that the invention of Larson et al is directed to a system/method that solves a different problem of rendering the data after it is in the register file and what data to pass from the register file to the rendering engine. The claimed invention is directed to improving the loading of the data into the register file in more efficient manner. The examiner also disagrees because Larson et al suggests that "a host processor generates a display list that includes **only the values necessary** for rendering a primitive. The graphics controller (or processor) includes a **register file for receiving the display list** either directly from the host or from system memory." (Abstract). Clearly, Larson et al also teaches to improving the loading of the data into the register file by only transfer the shortened display list that includes **only the values necessary** for rendering a primitive in order to load the data into the register file in more efficient manner.

Third, applicant argues that the disclosure of Larson et al does not suggest or contemplate use of a partition look-up table to generate the addresses to the register file. Here applicant argues limitations that are not in the claims. The Specification is not the measure of invention. Therefore, limitations contained therein can not be read into the claims for the purpose of avoiding the prior art. In re Sporck, 55 CCPA 743, 386 F .2d 924, 155 USPQ 687 (1968).

Finally, applicant argues that Larson et al has no suggestion of unique instruction format that provides the instruction, the parameters to load an the partition address. Similar as above third point, applicant also argues limitations that are not in the claims. The Specification is not the measure of invention. Therefore, limitations contained therein can not be read into the claims for the purpose of avoiding the prior art. In re Sporck, 55 CCPA 743, 386 F .2d 924, 155 USPQ 687 (1968). Therefore, applicant's arguments are not deemed to be persuasive.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be

calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Responses

8. Responses to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231.

If applicant desires to fax a response, (703) **308-9051(52)** may be used for formal communications or (703) **308-6606** for informal or draft communications.

Please label "PROPOSED" or "DRAFT" for informal facsimile communications. For after final responses, please label "AFTER FINAL" or "EXPEDITED PROCEDURE" on the document.

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

Inquires

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Kee M. Tung** whose telephone number is (703) **305-9660**. The examiner can normally be reached on **Monday - Thursday** from **7:30 am to 5:00 pm**. The examiner can also be reached on alternate **Friday**.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Matt Kim**, can be reached on (703) **305-3821**.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) **305-3800**.

April 6, 1999

Kee M. Tung
Primary Examiner
Art Unit 2773